REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-12 are pending in the present application. Claims 1 and 5 are amended by the present amendment.

In the outstanding Office Action, the drawings were objected to; the specification was objected to; Claims 1, 2, and 10 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,523,136 to Higashida; Claims 3, 4, 11, and 12 were rejected under 35 U.S.C. § 103(a) as unpatentable over Higashida; and Claims 5-9 were rejected under 35 U.S.C. § 103(a) as unpatentable over Higashida in view of U.S. Patent No. 5,566,303 to Tashiro et al. (herein "Tashiro").

Regarding the objection to the drawings, Figure 6 is amended to show the internal control signal generator 15, in light of comments in the outstanding Office Action. Accordingly, it is respectfully requested that objection be withdrawn.

Further, regarding the objection to the specification, the specification is amended in light of suggestions in the outstanding Office Action. Accordingly, it is respectfully requested that objection also be withdrawn.

Claims 1, 2, and 10 were rejected under 35 U.S.C. § 102(e) as anticipated by Higashida. Applicant respectfully traverses that objection.

Claim 1 is directed to a system LSI formed on one chip including a storage circuit, processor circuit with a program counter, and a peripheral circuit including a function block. In addition, the system LSI includes a selection means for optionally selecting one output of the program counter, the computing unit and the register in the processor circuit, at least one output of the storage circuit, and one output of a plurality of internal signals in the peripheral circuit including an output of the functional block. Further, the system LSI also includes a

10

selection control means for controlling selection of a result signal from any operation process in any place of the processor circuit, the storage circuit and the peripheral circuit, based on a selection signal which is supplied from the outside of the system LSI via an external terminal.

Applicant respectfully submits that Higashida does not teach or suggest the claimed selection means or the claimed selection control means. Further, applicant respectfully traverses the statement in the outstanding Office Action that Higashida discloses a selection means in column 1, lines 22-37, column 7, lines 15-30, and Figures 2 and 3.[1] Applicant respectfully submits that Higashida does not describe any selection means in column 1. Further, in column 7, Higashida indicates that an instruction execution processing portion 2C transmits a control signal via a CPU internal bus 2D. However, Higashida does not teach or suggest "selection means for optionally selecting one of the outputs" or "selection control means for controlling selection of a result signal."

In particular, Higashida shows a detailed configuration of a CPU core in Figure 2 and shows a detailed configuration of a multiplexer in Figure 3. However, the multiplexer 8 selects any of the signals on an internal bus corresponding to test mode instruction signal TP1 and TP2 that are externally supplied via a signal input terminal 9, which is different then the claimed invention which controls the selection means by the selection control means internally provided in the LSI. Thus, applicant respectfully submits that Higashida does not teach or suggest a system LSI that includes "selection control means for controlling selection of a result signal from any operation process in any place of said processor circuit, said storage circuit and said peripheral circuit, on the basis of a selection signal which is supplied from an outside of said system LSI via an external terminal," as in Claim 1.

Further, applicant respectfully traverses the statement in the outstanding Office Action that Higashida performs a "selector control by way of a signal via an external

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[1] Office Action mailed December 8, 2003, at page 4, lines 3-5.

terminal."[2] Applicant respectfully submits that <u>Higashida</u> does not teach or suggest a selection control means that outputs the selection control signal to the selection means responsive to the external selection signal. As indicated by Fig. 1, <u>Higashida</u> discloses a DSU-adapted debug device 20 which is externally provided and controls DSU 2A via a pin terminal 10 of the LSI. Hence, it is respectfully submitted that <u>Higashida</u> does not teach or suggest a system LSI that includes a "selection control means for controlling selection of a result signal from any operation process in any place of said processor circuit, said storage circuit and said peripheral circuit," as in Claim 1.

Accordingly, it is respectfully submitted that independent Claim 1 and claims depending therefrom patentably define over <u>Higashida</u>.

Claims 3, 4, 11, and 12 were rejected under 35 U.S.C. § 103(a) as unpatentable over <u>Higashida</u>, and Claims 5-9 were rejected under 35 U.S.C. § 103(a) as unpatentable over <u>Higashida</u> in view of <u>Tashiro</u>. Applicant respectfully traverses those rejections.

Claims 3-9, 11, and 12 depend on Claim 1, which as discussed above is believed to patentably define over <u>Higashida</u>. Further, it is respectfully submitted <u>Tashiro</u> also does not teach or suggest the features recited in the independent claims. Accordingly, it is respectfully requested those rejections also be withdrawn.

Accordingly, it is respectfully submitted that independent Claim 1 and claims depending therefrom are allowable.

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[2] Office Action mailed December 8, 2003, at page 4, line 5.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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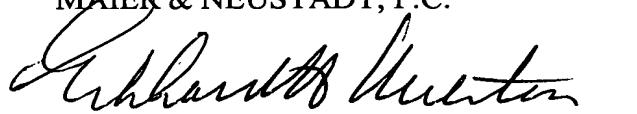
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13